

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Original to parent) A method performed by a data processing system
2 having a memory, comprising the steps of:
3 parsing a text description of a circuit, said text description stored in the
4 memory, said text description including a loop with a delayed signal assignment
5 having a delay value;
6 translating said text description into a digital circuit representation in said
7 memory, said digital circuit representation including a pipeline; and
8 setting a latency of said pipeline equal to said delay value.
- 1 2. (Original to parent) The method of claim 1, wherein said loop further
2 includes N wait statements, where N is greater than zero, said method further
3 comprising the step of setting an initiation interval of said pipeline equal to N.
- 1 3. (Original to parent) The method of claim 1, wherein said text
2 description is written in Verilog and said delayed signal assignment uses a Verilog
3 “#” operator.
- 1 4. (Original to parent, amended twice) The method of claim 2[3],
2 wherein said wait statements transition on[use] Verilog “@posedge” statements.
- 1 5. (Original to parent, amended twice) The method of claim 2[3],
2 wherein said wait statements transition on[use] Verilog “@negedge” statements.

1 6. (Original to parent, amended once) The method of claim 2[1], wherein
2 said text description is written in VHDL, said delayed signal assignment uses a
3 VHDL “_after_” clause, and said wait statements use VHDL “wait” statements.

1 7. (Original to parent) A method, performed by a data processing system
2 having a memory of building a digital circuit representation including a pipeline
3 in the memory from a textual description of a loop, comprising the steps of:
4 identifying a loop carry dependency in said loop;
5 identifying a producer operation of said loop carry dependency;
6 identifying a consumer operation of said loop carry dependency;
7 determining a number, n, of cycles within which said producer operation
8 must be scheduled after said consumer operation;
9 instantiating a placeholder node in said memory;
10 node-locking said placeholder node so that it must be scheduled n cycles
11 after said consumer operation; and
12 constraining said producer operation to be scheduled before said
13 placeholder node.

1 8. (Original to parent) The method of claim 7, wherein the step of node-
2 locking said placeholder node further comprises the step of creating a template
3 structure in said memory which includes said placeholder node and said consumer
4 operation.

1 9. (Original to parent) The method of claim 8,
2 wherein said producer operation is included in a second template structure
3 in said memory, and

4 wherein the step of constraining said producer operation further comprises
5 the step of constraining said second template structure to be scheduled before said
6 template structure.

1 10. (Original to parent, amended once) The method of claim 7, wherein n
2 is equal to an initiation interval of said pipeline multiplied by a number of
3 iterations of said loop which execute before data produced by said producer
4 operation is consumed by said consumer operation.

1 11. (Original to parent) A method, performed by a data processing
2 system having a memory, of building a digital circuit representation in said
3 memory, said digital circuit representation including a pipeline derived from a
4 textual description of a loop, said method comprising the steps of:
5 identifying an access dependency of said loop;
6 identifying a first access operation of said access dependency;
7 identifying a second access operation of said access dependency;
8 determining a number, n, of cycles within which said second access
9 operation must be scheduled after said first access operation;
10 instantiating a placeholder node in said memory;
11 node-locking said placeholder node so that it must be scheduled n cycles
12 after said first access operation; and
13 constraining a scheduling order of said second access operation and said
14 placeholder node.

1 12. (Original to parent, amended once) The method of claim 11,
2 wherein said first access operation is chosen from a[the] group of access
3 operations including a memory read, a memory write, a signal write and a port
4 write,

5 said second access operation is chosen from the group of access operations
6 including a memory read, a memory write, a signal read, a signal write, a port read
7 and a port write, and
8 the step of constraining said scheduling order of said second access
9 operation and said placeholder node further includes the step of forcing said
10 second access operation to be scheduled before said placeholder node.

1 13. (Original to parent, amended once) The method of claim 11,
2 wherein said first access operation is chosen from a[the] group of access
3 operations including a memory read, a memory write, a signal read, a signal write,
4 a port read and a port write,
5 said second access operation is chosen from the group of access operations
6 including a memory read, a memory write, a signal write and a port write, and
7 the step of constraining said scheduling order of said second access
8 operation and said placeholder node further includes the step of forcing said
9 second access operation to be scheduled before said placeholder node.

1 14. (Original to parent, amended once) The method of claim 11,
2 wherein said first access operation is chosen from a[the] group of access
3 operations including a signal read and a port read,
4 said second access operation is chosen from the group of access operations
5 including a signal read and a port read, and
6 the step of constraining said scheduling order of said second access
7 operation and said placeholder node further includes the step of forcing said
8 second access operation to be scheduled simultaneous with, or before said
9 placeholder node.

1 15. (Original to parent) The method of claim 11, wherein the step of
2 constraining said scheduling order of said second access operation and said
3 placeholder node further includes the step of forcing said second access operation
4 to be scheduled before said placeholder node.

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1 16. (Original to parent) The method of claim 11, wherein the step of node-
2 locking said placeholder node further includes the step of creating a template
3 which includes said placeholder node and said first access operation.

1 17. (Original to parent) The method of claim 11, wherein n is equal to an
2 initiation interval of said pipeline multiplied by a number of iterations of said loop
3 which execute between said first access operation and said second access
4 operation.

1 18. (Original to parent) A system for building, in a memory, a digital
2 circuit representation which implements the behavior of a text description in said
3 memory, said system having a processor coupled to a memory unit wherein said
4 processor is programmed to perform logic processing, said system comprising:
5 parsing logic for parsing said text description into a parsed text
6 description, said text description including a loop with a delayed signal
7 assignment having a delay value;
8 translating logic for translating said parsed text description into said digital
9 circuit representation, said digital circuit including a pipeline; and
10 latency setting logic for setting a latency value of said pipeline to be said
11 delay value of said delayed signal assignment.

1 19. (Original to parent) A system as described in claim 18, wherein said
2 pipeline implements said loop.

1 20. (Original to parent) A system as described in claim 19, wherein said
2 loop further includes a number, n, of wait statements, said system further
3 comprising initiation interval setting logic for setting an initiation interval of said
4 pipeline to be equal to n.

1 21. (Original to parent) A computer program product comprising:
2 a computer usable medium having computer readable code embodied
3 therein for building a digital circuit representation from a text description of a
4 digital circuit, the computer program product comprising:
5 computer readable program code devices configured to cause a computer
6 to effect parsing said text description, said text description including a loop with a
7 delayed signal assignment having a delay value;
8 computer readable program code devices configured to cause a computer
9 to effect translating said text description into said digital circuit representation
10 including a pipeline; and
11 computer readable program code devices configured to cause a computer
12 to effect setting a latency of said pipeline equal to said delay value.

1 22. (Original to parent) The computer program product of claim 21
2 wherein said loop further includes N wait statements, where N is greater than
3 zero, said computer program product further comprising computer readable
4 program code devices configured to cause a computer to effect setting an
5 initiation interval of said pipeline equal to N.

1 23. (New) A method performed by a data processing system having a
2 memory, comprising the steps of:

3 parsing a text description of a circuit, said text description stored in the
4 memory, said text description including a loop with N wait statements, where N is
5 greater than zero;
6 translating said text description into a digital circuit representation in said
7 memory, said digital circuit representation including a pipeline; and
8 setting an initiation interval of said pipeline equal to N.

1 24. (New) The method of claim 23, wherein the wait statements are
2 VHDL wait statements.

1 25. (New) The method of claim 23, wherein the wait statements transition
2 on Verilog HDL @posedge statements.

1 26. (New) The method of claim 23, wherein the wait statements transition
2 on Verilog HDL @negedge statements.

1 27. (New) A system for building, in a memory, a digital circuit
2 representation which implements the behavior of a text description in said
3 memory, said system having a processor coupled to a memory unit wherein said
4 processor is programmed to perform logic processing, said system comprising:
5 parsing logic for parsing said text description into a parsed text
6 description, said text description including a loop with N wait statements, where
7 N is greater than zero;
8 translating logic for translating said parsed text description into said digital
9 circuit representation, said digital circuit including a pipeline; and
10 initiation interval setting logic for setting an initiation interval of said
11 pipeline equal to N.

1 28. (New) The system of claim 27, wherein the wait statements are VHDL
2 wait statements.

1 29. (New) The system of claim 27, wherein the wait statements transition
2 on Verilog HDL @posedge statements.

1 30. (New) The system of claim 27, wherein the wait statements transition
2 on Verilog HDL @negedge statements.

1 31. (New) A computer program product comprising a computer usable
2 medium having computer readable code embodied therein for building a digital
3 circuit representation from a text description of a digital circuit, the computer
4 program product comprising:
5 computer readable program code devices configured to cause a computer
6 to effect parsing said text description, said text description including a loop with
7 N wait statements, where N is greater than zero;
8 computer readable program code devices configured to cause a computer
9 to effect translating said text description into said digital circuit representation
10 including a pipeline; and
11 computer readable program code devices configured to cause a computer
12 to effect setting an initiation interval of said pipeline equal to N.

1 32. (New) The method of claim 31, wherein the wait statements are
2 VHDL wait statements.

1 33. (New) The method of claim 31, wherein the wait statements transition
2 on Verilog HDL @posedge statements.

1 34. (New) The method of claim 31, wherein the wait statements transition
2 on Verilog HDL @negedge statements.

1 35. (New) The method of claim 1, wherein said loop further includes N
2 clock statements, where N is greater than zero, said method further comprising the
3 step of setting an initiation interval of said pipeline equal to N.

1 36. (New) A system as described in claim 18, wherein said loop further
2 includes a number, n, of clock statements, said system further comprising
3 initiation interval setting logic for setting an initiation interval of said pipeline to
4 be equal to n.

1 37. (New) The computer program product of claim 21 wherein said loop
2 further includes N clock statements, where N is greater than zero, said computer
3 program product further comprising computer readable program code devices
4 configured to cause a computer to effect setting an initiation interval of said
5 pipeline equal to N.

1 38. (New) A method performed by a data processing system having a
2 memory, comprising the steps of:
3 parsing a text description of a circuit, said text description stored in the
4 memory, said text description including a loop with N clock statements, where N
5 is greater than zero;
6 translating said text description into a digital circuit representation in said
7 memory, said digital circuit representation including a pipeline; and
8 setting an initiation interval of said pipeline equal to N.

1 39. (New) A system for building, in a memory, a digital circuit
2 representation which implements the behavior of a text description in said
3 memory, said system having a processor coupled to a memory unit wherein said
4 processor is programmed to perform logic processing, said system comprising:
5 parsing logic for parsing said text description into a parsed text
6 description, said text description including a loop with N clock statements, where
7 N is greater than zero;
8 translating logic for translating said parsed text description into said digital
9 circuit representation, said digital circuit including a pipeline; and
10 initiation interval setting logic for setting an initiation interval of said
11 pipeline equal to N.

1 40. (New) A computer program product comprising a computer usable
2 medium having computer readable code embodied therein for building a digital
3 circuit representation from a text description of a digital circuit, the computer
4 program product comprising:
5 computer readable program code devices configured to cause a computer
6 to effect parsing said text description, said text description including a loop with
7 N clock statements, where N is greater than zero;
8 computer readable program code devices configured to cause a computer
9 to effect translating said text description into said digital circuit representation
10 including a pipeline; and
11 computer readable program code devices configured to cause a computer
12 to effect setting an initiation interval of said pipeline equal to N.